SANTA CLARA UNIVERSITY

Funded Ph.D. or Master's Student Position

About the Open Position: Dr. Hoeseok Yang, an Associate Professor in the Department of Electrical and Computer Engineering at Santa Clara University (SCU), is currently seeking a motivated prospective Master's or Doctoral (Ph.D.) student in the field of **Hardware-Software Co-Design of Large Language Models (LLMs)**. We previously applied the Hardware-Software Co-Design methodology to various domains such as low-power systems or safety-critical systems. The current focus has shifted towards LLMs as the model-architecture co-design of LLMs is a big open research problem for both academia and industry.

About SCU: Located in the heart of Silicon Valley, SCU blends high-tech innovation with a social consciousness grounded in the Jesuit educational tradition. Consistently recognized as one of the top universities in the nation, SCU is committed to leaving the world a better place. SCU pursues new technology, encourages creativity, engages with our communities, and shares an entrepreneurial mindset. The goal is to help shape the next generation of leaders and global thinkers. More information can be found at https://www.scu.edu/aboutscu/. Students benefit from the thriving Silicon Valley market for summer internships or after graduation.

About our Graduate Programs: We are featured by providing a funded Master's degree program to talented candidates in addition to the Ph.D. program in Electrical and Computer Engineering.

Qualifications

- Expected to have a Bachelor's or Master's (necessary for Ph.D.) degree in Electrical and Computer Engineering, Computer Science and Engineering, or closely related fields,
- Knowledge of embedded system design and computer architecture at the undergraduate level is essential,
- Strong programming experience in Python and C/C++ required,
- Experience with deep learning modeling frameworks, such as TensorFlow or PyTorch, is preferred,
- Experience with GPU programming (CUDA or OpenCL) or Hardware Description Language (Verilog or VHDL) is a plus, and
- Good verbal and written English communication skills required.

Expected Start Time: September 2024

Application: Interested candidates are invited to send the following documents to Dr. Yang (hoeseok.yang@scu.edu)

- a detailed CV and
- a statement of purpose outlining the research interests and career goals.

Santa Clara University
School of Engineering